Dual-Channel RAW and YUV Image Output CIS with 130dB DR and LFM for Automotive Applications

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***Abstract*—This paper presents a dual-channel RAW and YUV image output CMOS images sensor (CIS) with high dynamic range (HDR) and LED flicker mitigation (LFM). To achieve a simplified system configuration, low-cost and low-power consumption, we implemented the data path and image signal processing (ISP) block which can generate the RAW and YUV data simultaneously. To achieve HDR and LFM, we implemented a sub-pixel architecture in the proposed CIS. With the dual-channel RAW and YUV image output CIS, the power consumption was reduced by 34.5% compared with a conventional system based on using two sensors, one for RAW and the other for YUV. In addition, it achieved dynamic range of 105dB (w/LFM) and 130dB (w/o LFM).**

Keywords—CMOS Image Sensor, Automotive, dual-channel output, RAW and YUV, HDR, LFM

I. Introduction

A CMOS Image Sensor (CIS) for automotive applications needs to support high dynamic range (HDR) and LED flicker mitigation (LFM). Conventionally this is achieved by using multiple exposures or sub-pixel photodiodes [1-6]. As shown in Fig. 1, for automotive applications both RAW and YUV image data are needed for the detection and recognition of the external environment. Typically RAW image data is used for advanced driver-assistance systems (ADAS) and autonomous driving systems (AD), whereas YUV image data is used for infotainment applications such as the drive recorder and augmented reality (AR). To realize ADAS/AD and infotainment, separate CISs can be used to generate the RAW and YUV image, respectively. This architecture is easy to implement, but it doubles the system-level cost, complexity, and power consumption. To achieve the simplified system configuration, low-cost and low-power consumption, the proposed CIS outputs the RAW and YUV images simultaneously. Moreover, the proposed CIS achieved HDR and LFM by using the sub-pixel structure.

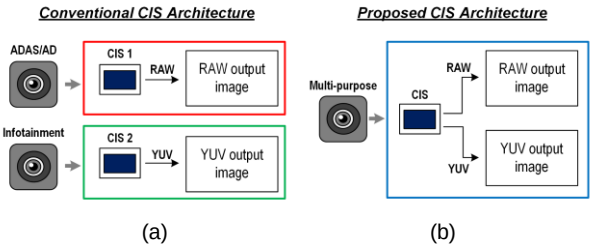


Fig. 1. (a) conventional and (b) proposed CIS architecture for the RAW and YUV outputs.

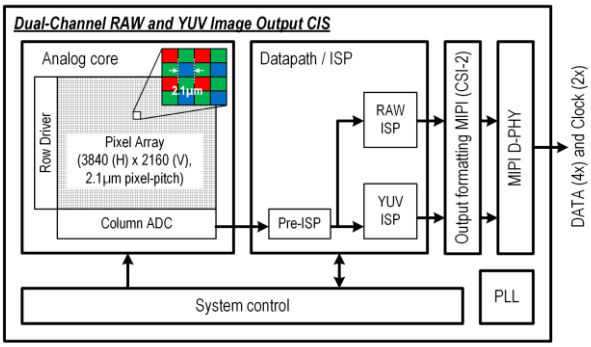
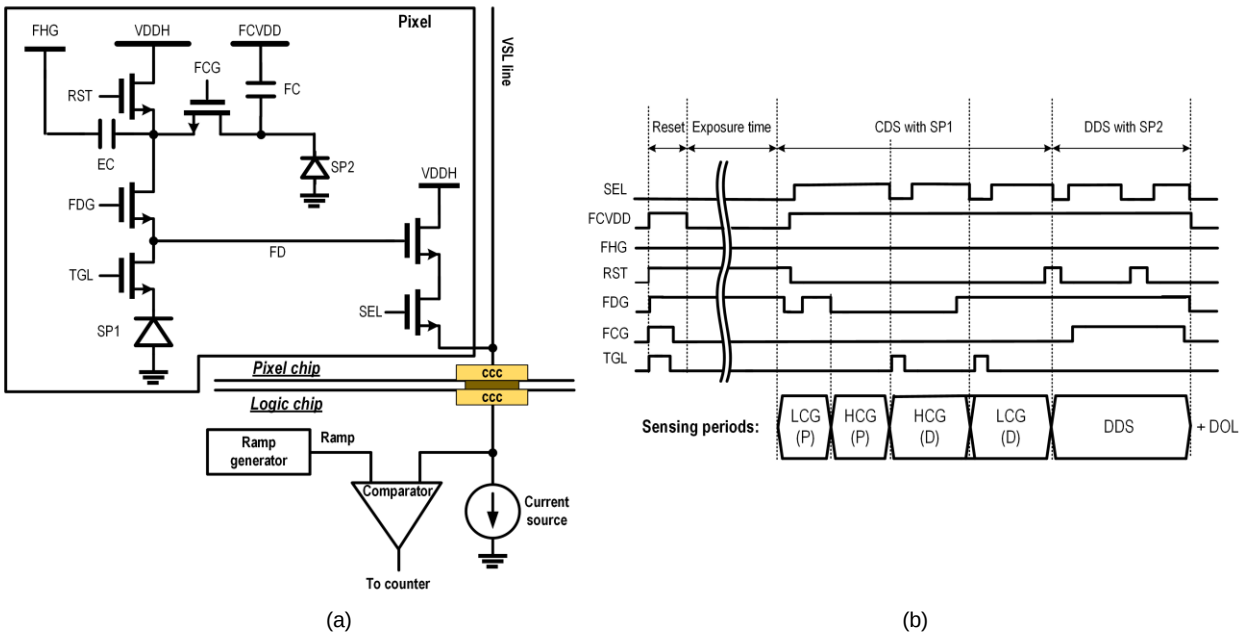


Fig. 2. The proposed system architecture of dual-channel RAW and YUV image output CIS.

II. Proposed Dual-Channel RAW and YUV Image Output CIS

A. System Architecture

Fig. 2 shows the proposed system architecture of the dual-channel RAW and YUV image output CIS. The CIS consists of the analog core block, the datapath/image signal processing (ISP) block, the output formatting MIPI (CSI-2) block, the MIPI D-PHY block which has 4-lane data and 2-lane clock-, the PLL and the system control blocks. The analog core block has a 3840 (H) x 2160 (V) pixel array (8.3Mpixel) with 2.1µm pixel-pitch, row driver and column analog-to-digital converter (ADC). The analog core block



(a) (b)

Fig. 3. (a) Pixel circuit diagram of sub-pixel architecture and (b) its timing diagram.

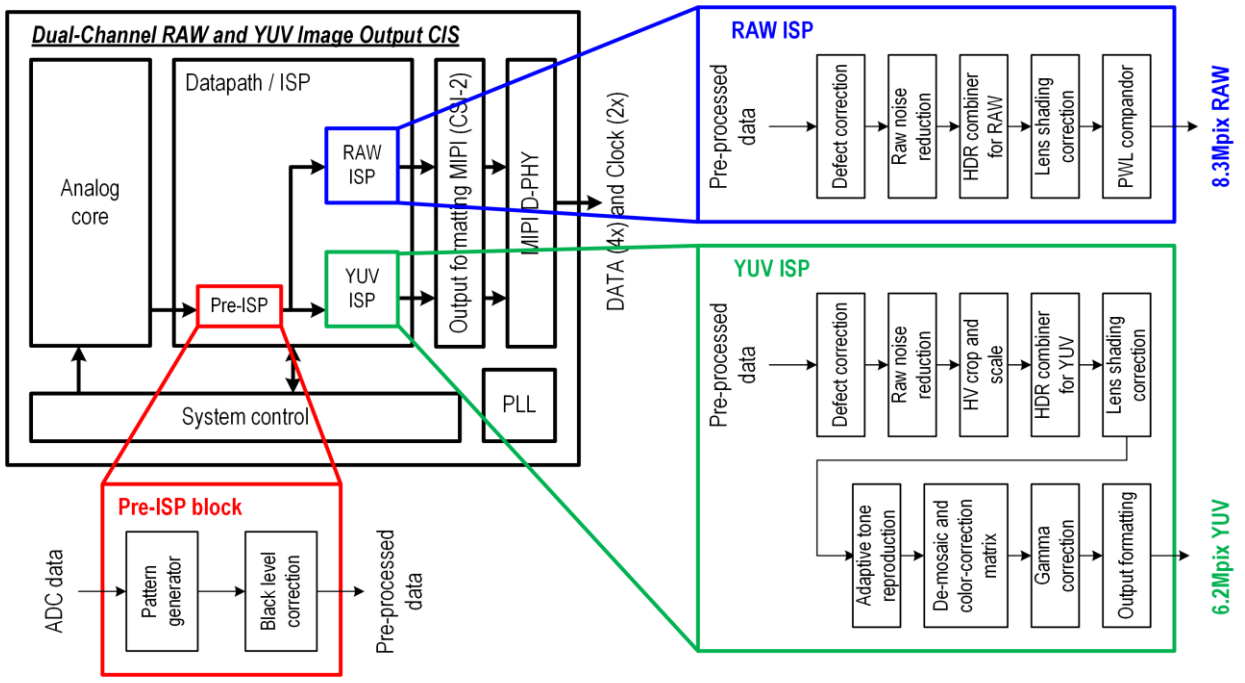


Fig. 4. Data processing pipeline for the RAW and YUV.

outputs the digital pixel values to the datapath/ISP block which consists of pre-ISP, RAW and YUV ISPs. The datapath/ISP block generates the two output data. The CSI-2 adaptively outputs the data on a single-port with 4-lanes or dual-ports with 2-lanes each via the MIPI D-PHY with the 30Hz frame rate.

B. Pixel Architecture and Timing Diagram

Fig. 3 shows the sub-pixel architecture which is connected to the current source and the comparator via the copper-copper connection (CCC). The pixel has 6 transistors, 2 photo diodes (SP1 for the high-sensitivity and SP2 for the low-sensitivity), and two capacitors (EC and FC). To achieve low-noise performance, the high-conversion gain capture (HCG) is done with the SP1. To achieve wide dynamic range, and keeping the high SNR, the low-conversion gain capture (LCG) is done with SP1 and EC by turning on the FDG transistor. To sense the high luminance, the double delta sampling capture (DDS) is done with SP2 and FC. For further increase of dynamic range, the SP1 is sensed again with the digital overlap short exposure time capture (DOL). The detailed operation of the pixel architecture is shown in Fig. 3. It shows the reset, exposure time, correlated double sampling readout with the SP1 (LCG and HCG), the DDS readout with SP2 and DOL. The P- and D-phases of each period (HCG, LCG, DDS, and DOL) are A/D converted through the current source, ramp generator, comparator, and counter. By combining all captures, the proposed CIS achieved

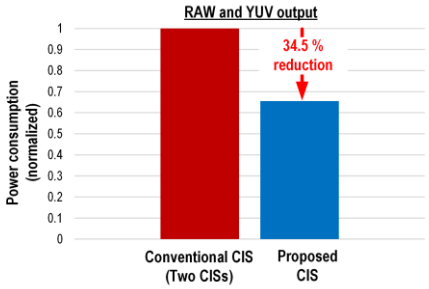


Fig. 5. Comparison of power consumption between two CISs (conventional) and propose CIS to output the RAW and YUV data.

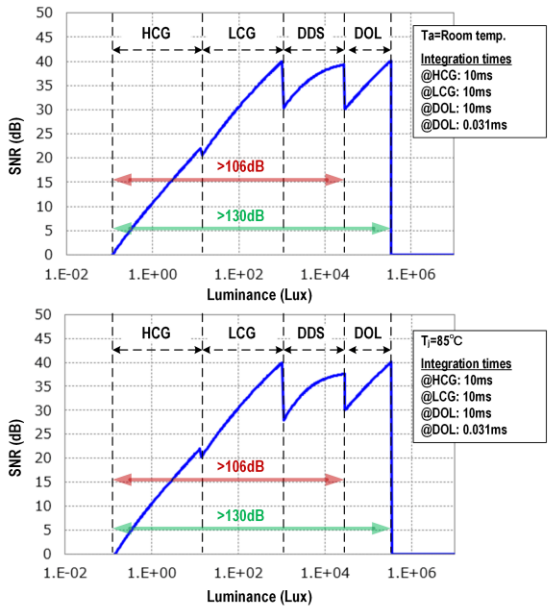


Fig. 6. HDR SNR curves at room temperature (T_a=RT) and high temperatures (T_j=85℃).

Fig. 7. Synthesized RAW and YUV image.

105dB (w/LFM) and 130dB (w/o LFM).

C. RAW and YUV Processing Pipeline

Fig. 4 shows the data processing pipeline for the RAW and YUV. The datapath/ISP block consists of the pre-ISP, RAW and YUV ISP blocks. When the Pre-ISP block receives the ADC data from the counter, the black level correction block subtracts the dark current and offset from the active region pixel data (pre-processed data). The pattern generator is used for the confirmation of the data processing pipeline. When the pre-ISP outputs the pre-processed data, the RAW and YUV ISP receive the data in parallel.

The RAW ISP consists of the defect correction, raw noise reduction, HDR combiner, lens shading correction, and PWL compandor. When the defect correction block detects the abnormal pixel values, it averages and corrects

TABLE I. PERFORMANCE SUMMARY

Lists	Unit	Specification
Process	-	Pixel chip 90 nm / logic chip 22nm, stacked BSI
Power supply	V	3.0 / 1.8 / 0.8
Pixel array	-	8.3Mpixel 3840 (H) × 2160 (V)
Image size	-	1/1.72-inch
Unit pixel size	-	2.1μm (H) × 2.1μm (V) (RYYCy or RGGB)
Max. frame rate @12bit	Hz	30 (RAW and YUV dual output)
Conversion gain @ HCG	μV/e-	176
Full-well capacity @ HCG	e-	2400
Noise @HCG and 85℃	e-rms	0.96
Dynamic range	dB	106 (with LFM) 130 (dynamic range priority)
Interface	-	MIPI CSI-2 serial output (Single port with 4-lanes / Dual port with 2-lanes per port)
Package	-	Plastic BGA 192pin, 11.85 x 8.66mm

it based on the neighboring pixel information. After noise filtering with the raw noise reduction block, the HDR combiner block combines four captures (HCG, LCG, DDS, and DOL) into one data over the luminance by using digital gain. Finally, the lens correction and PWL compandor compensates the lens shading and compresses the internal linear high resolution pixel values to the system requirement bit resolution and outputs the 8.3Mpixel data.

The YUV ISP also receives the pre-processed data. The defect pixel correction and raw noise reduction blocks process the data similar to the RAW ISP. To optimize the power consumption, the HV crop and scale blocks crops and rescales the pre-processed data to 6.2Mpixel data. After the lens shading correction, same as the RAW ISP block, the adaptive tone reproduction block compresses the data to lower bit resolution while preserving local contrast in the image to optimize the image quality for human vision perception. The de-mosaic and color-correction matrix blocks interpolate the pixel data and improves the color reproduction. The gamma correction block enables further contrast adjustment of the image data. The output formatting block filters and corrects the data to output the 6.2Mpixel YUV image with high image quality. To optimize the power consumption of the proposed CIS, standard- and low-threshold devices were adaptively used in the low- and high-speed logic respectively.

III. EVALAUTION RESULTS

Fig. 5 shows the comparison of power consumption between two conventional CISs and the proposed CIS that can output RAW and YUV. To compare the power consumption, the power consumptions of RAW and YUV output were calculated separately and simultaneously with the same proposed CIS. Compared with the separated RAW and YUV output configuration, dual output mode can reduce the power consumption by 34.5%.

Fig. 6 shows the HDR SNR curves at room temperature and high temperatures (T_j=85℃) over the luminance. The exposure time for HCG and LCG, and DDS were set to 10ms. The dynamic range from the HCG, LCG and DDS

captures is over 106 dB at T_a=RT and T_j=85℃ and the minimum SNR is 27.9dB in the knee-point between LCG and DDS. With the DOL operation (0.031ms exposure time), the dynamic range is larger than 120dB in both temperature conditions.

Fig. 7 shows the synthesized RAW and YUV image. The proposed CIS successfully outputs the RAW and YUV images in parallel with 30Hz frame rate. Table I shows the performance summary.

IV. Conclusion

This paper presented a dual-channel RAW and YUV image output CIS to achieve simplified system configuration, low-cost and low-power consumption with HDR and LFM. With the dual-channel RAW and YUV output, the proposed CIS reduced the power consumption by 34.5% compared with the conventional CIS. In addition, the proposed CIS achieved dynamic range 105dB (w/LFM) and 130dB (w/o LFM) while keeping the knee-point SNR (over 25dB) at T_j=85℃.

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